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10/734,763	12/11/2003	Rabin Sugumar	004-8639	1964

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	04/17/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,763	SUGUMAR ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-18,20-23 and 25-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,6,8-18,20-23,25-31 and 33-35* is/are rejected.

7)☒ Claim(s) *7,32 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 26 recites the limitation "the fetch group" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims1,15,17, 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair (patent No. 6,195,746) in view of Gaertner (patent No. 6,237,076).

5. Nair taught the invention substantially as claimed including a data processing ("DP") system comprising: As per claims (1,15,20,) Nair taught if a dependency exists one instruction and a result stored in a register of differing register type the register type specifiers were converted to match the type specifier in the instruction (e.g., see fig. 5 and col. 6, line 53-col. 8, line 26 and, col. 9, lines 7-60)[Nair taught the changing of register type specifiers changes the execution unit and associated register. The

specifier is allocated where the execution unit are of various types is different register widths (e.g., see col. 3, line 50-col. 4, line 32) and Nair taught some execution units performing single precision operations and others performing double precision operations (e.g., see col. 7, lines 26-52). Nair provided a CAST instruction for dynamically converting register type specifier , looking up the specifier type for the source operand, where when the source register specifier type was different from the target register specifier type, the type target register specifier are converted to match the type specifier of the field of the instruction e.g., see col. 5, lines 1-34).

6. Nair taught that the instructions that converted register specifier types comprised LOAD, STORE and CAST instruction (e.g., see col. 9, lines 21-60). Here data in the register designated by the source in a load or CAST instruction would have been generated and stored in the source register by another (previous) instruction in the course of processing of instructions. Therefore since Nair provided for substitution of register specifier in any case where the type of the specifiers were different then, it would have been obvious to one of ordinary skill that in the Nair teachings during processing of instructions (e.g., single precision and double precision floating point instructions and fixed point instructions) the LOAD or CAST from between a greater width producer instruction (executed in one execution unit) and a lesser width consumer instruction (executed in another execution unit), Nair would have substituted for execution a greater width source register specifier for a lesser width source register specified by lesser width consumer instruction.

7. Nair did not expressly detail (claim 1,15,17,20-22) processor executing the greater width producer instruction and placing a result of the execution in the greater width source register and the processor executing the lesser width consumer instruction using the greater width source register the replacing of a greater width source register specifier for a lesser width source register specifier. Gaertner however taught this limitation (e.g., see fig. 1, col. 3, lines 31-col. 4, lines 16)[as to the replacing specifiers the logical registers are renamed and where a 32 bit register is renamed to a 64 bit register when the 32 bit instruction depends on result of a 64 bit instruction also renaming also occurs when a 64 bit instruction uses the destination of a 32 bit instruction].

8. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Nair and Gaertner. Both references were directed toward the problems of executing instructions of different widths in a DP system. One of ordinary skill would have been motivated to incorporate the Gaertner teachings of using the wide 64 bit register when a 32 bit instruction depended on a 64 bit instruction at least to eliminating the need to use different width registers and therefore reducing the amount of logic need to control storage of the data (e.g., see col. 1, lines 3-23 of Gaertner).

9. Further as to claim 15,20, since the use of instruction with greater width source and destination operands (e.g., double precision) and instructions with lesser width source and destination operands (e.g., single precision) and the Nair system provided register type specifiers for each register including the register type providing information such as register size and replaced register specifiers when the specifier type between

source and target do not match(as discussed above) In the Nair teachings a consumer instruction comprises a larger width source register specifier than the producer instruction. One of ordinary skill would have been motivated replace the lesser width source register specifier of the second (i.e., consumer) instruction with the greater width source register specifier so that the instruction would be performed properly with the proper size registers.

10. As per claim 17,22 Nair taught substituting the greater width register includes setting an indication that the lesser width source register is to be replaced by the greater width register (e.g., see col. 5, lines 1-67 and col. 6, line 53-col. 7, line 52)[the type indicator indicates to the system when a register is to be replaced when the source and target types (such as sizes) are different].

11. Nair taught when there is a type difference between operands (such as different width operands) if the types are not supported by the architecture an exception should be generated (e.g., see col. 7,lines 2-17). Since the exception in the pipeline would have provided a need to wait for the processing of the exception one of ordinary skill would have been motivated to stall the pipeline at least to ensure the data for processing and processing sequence is correct. This provide for logic (the scope provides for any type of logic including one of software or hardware) for producing an exception which would have prevented the one instruction from being delivered for execution if its dependency depends between an instruction in the fetch group and both

an active lesser width produce instruction and a active greater width producer instruction.

12. As per claim 21, Nair taught when there is a type difference between operands (such as different width operands) if the types are not supported by the architecture an exception should be generated (e.g., see col. 7,lines 2-17). Since the exception in the pipeline would have provided a need to wait for the processing of the exception one of ordinary skill would have been motivated to stall the pipeline at least to ensure the data for processing and processing sequence is correct.

Claim Rejections - 35 USC § 102

13. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

14. Claim 4,18,23 is rejected under 35 U.S.C. 102(b) as being anticipated by Prabu (patent No. 6,463,525).

15. As to the limitations of claim 4,23 Prabu taught if a dependency exists between a lesser width producer instruction and a greater width consumer instruction, substituting plural instructions [a double precision operation is performed on data stored by a plural single precision operations] (e.g., see col. 3, lines 8-43). Prabu taught the plural

instructions substituted for the greater width consumer instruction include a first instruction to merge plural lesser width registers aliased on to a first greater width source register of the greater width consumer instruction(merge% f0,f1,→% d0) the plural lesser width registers to be merged into a first temporary register; a second instruction to merge plural lesser width registers aliased onto a second greater width source register of the greater width consumer instruction (merge% f2,f3,→% d2), the plural lesser width registers to be merged into a second temporary register; and a third instruction to execute the greater width consumer instruction (fadd % d0,% d2,% d4) as executed with logic for designating and using the first temporary register and the second temporary register as source registers (e.g,. see , fig.2 and col. 4, lines 32-67 and col. 5, lines 16-44).[Since the data in f0,f1,f2,f3 are all 32 bit data it would have required an instruction could store 32 data and/or produce a 32 bit result therefore the source instruction would have had to have been a lesser width or 32 bit instruction where the addition implemented by the fadd was a 64 bit add or a greater width consumer instruction].

16. As per claim 18, Prabhu taught three instruction that together perform the operation of merging single precision registers that are mapped to act as a double precision register and performing double precision operations comprising plural operands on the data (e.g., see col. 4, lines 6-31).

Claim Rejections - 35 USC § 103

17. Claims 2,3,6,8-10,16,25,27-30, 31,33-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair in view of Gaertner and Prabu (patent No. 6,463,525).

18. Nair taught the invention substantially as claimed including a data processing ("DP") system comprising: As per claims (1,6,15,20,23,31) Nair taught if a dependency exists one instruction and a result stored in a register of differing register type the register type specifiers were converted to match the type specifier in the instruction (e.g., see fig. 5 and col. 6, line 53-col. 8, line 26 and, col. 9, lines 7-60)[Nair taught the changing of register type specifiers changes the execution unit and associated register. The specifier is allocated where the execution unit are of various types is different register widths (e.g., see col. 3, line 50-col. 4, line 32) and Nair taught some execution units performing single precision operations and others performing double precision operations (e.g., see col. 7, lines 26-52). Nair provided a CAST instruction for dynamically converting register type specifier , looking up the specifier type for the source operand, where when the source register specifier type was different from the target register specifier type, the type target register specifier are converted to match the type specifier of the field of the instruction e.g., see col. 5, lines 1-34).

19. Nair taught that the instructions that converted register specifier types comprised LOAD, STORE and CAST instruction (e.g., see col. 9, lines 21-60). Here data in the register designated by the source in a load or CAST instruction would have been generated and stored in the source register by another (previous) instruction in the course of processing of instructions. Therefore since Nair provided for substitution of

register specifier in any case where the type of the specifiers were different then, it would have been obvious to one of ordinary skill that in the Nair teachings during processing of instructions (e.g., single precision and double precision floating point instructions and fixed point instructions) the LOAD or CAST from between a greater width producer instruction (executed in one execution unit) and a lesser width consumer instruction (executed in another execution unit), Nair would have substituted for execution a greater width source register specifier for a lesser width source register specified by lesser width consumer instruction.

20. Nair did not expressly detail (claim 6,20,31) processor executing the greater width producer instruction and placing a result of the execution in the greater width source register and the processor executing the lesser width consumer instruction using the greater width source register the replacing of a greater width source register specifier for a lesser width source register specifier. Gaertner however taught this limitation (e.g., see fig. 1, col. 3, lines 31-col. 4, lines 16)[as to the replacing specifiers the logical registers are renamed and where a 32 bit register is renamed to a 64 bit register when the 32 bit instruction depends on result of a 64 bit instruction also renaming also occurs when a 64 bit instruction uses the destination of a 32 bit instruction].

21. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Nair and Gaertner. Both references were directed toward the problems of executing instructions of different widths in a DP system. One of ordinary skill would have been motivated to incorporate the Gaertner teachings of using the wide 64 bit

register when a 32 bit instruction depended on a 64 bit instruction at least to eliminating the need to use different width registers and therefore reducing the amount of logic need to control storage of the data (e.g., see col. 1, lines 3-23 of Gaertner).

22. As to the limitations of claim 6, 25,31,33 Nair did not specifically detail substituting an plural instructions for an instruction when a dependency between instructions Prabu taught if a dependency exists between a lesser width producer instruction and a greater width consumer instruction, the processor substituting plural instructions [a double precision operation is performed on data stored by a plural single precision operations and executing the instructions] (e.g., see col. 3, lines 8-43), and col. 4, line 6-col. 5, lines 44) (merge% f0,f1,→% d0) (merge% f2,f3,→% d2), (fadd % d0,% d2,% d4) (e.g., see , fig.2 and col. 4, lines 32-67 and col. 5, lines 16-44).[Since the data in f0,f1,f2,f3 are all 32 bit data it would have required an instruction could store 32 data and/or produce a 32 bit result therefore the source instruction would have had to have been a lesser width or 32 bit instruction where the addition implemented by the fadd was a 64 bit add or a greater width consumer instruction].

23. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Nair and Prabhu. Both references were directed to the problems of processing instructions with registers of plurality of widths (e.g., see col.3 lines 8-12 of Prabhu and col. 1, line 46-col. 2, line 18 of Nair). One of ordinary skill would have been motivated to incorporate the Prabhu teachings of substituting plural single precision

instructions for a double precision instruction to facilitates efficiently processing of the double precision instruction when the source operands were stored in single precision registers.

24. As per claims 2, 8,9,16, 28,31,33 Nair taught the greater width source register substituted for the lesser width source register is the greater width register onto which the lesser width source register is aliased, and setting an indication (e.g., see col. 5, lines 1-54).

25. Also, Prabhu taught the greater width source register substituted for the lesser width source register is the greater width register onto which the lesser width source register is aliased, and setting an indication (e.g., see col. 3, lines 15-43).

26. As per claim 3,17,22,27 Nair taught substituting the greater width register includes setting an indication that the lesser width source register is to be replaced by the greater width register (e.g., see col. 5, lines 1-67 and col. 6, line 53-col. 7, line 52)[the type indicator indicates to the system when a register is to be replaced when the source and target types (such as sizes) are different].

27. As per claim 10, Prabhu taught three instructions that together perform the operation of merging single precision registers that are mapped to act as a double precision register and performing double precision operations comprising plural operands on the data (e.g., see col. 4, lines 6-31).

28. As to the further limitations of claim 29, 30,34,35 the grouping of the fetching of instructions as a group was well known in the art at the time of the claimed invention and one of ordinary skill would have been motivated to fetch plural instructions used as

described above as group at least to speed fetching of instructions versus taking the time to fetech each instruction individually.

29. Claims 11,12,13,14,are rejected under 35 U.S.C. 103(a) as being unpatentable over Nair,Gaertner, and Prabhu as applied to claims 6 above, and further in view of Yeager (patent No. 6,216,200)(cited in last office action).

30. Prabu taught if a dependency exists between a lesser width producer instruction and a greater width consumer instruction, substituting plural instructions [a double precision operation is performed on data stored by a plural single precision operations] (e.g., see col. 3, lines 8-43).

31. Yeager taught (claims 11,12,) generating a first register mask identifying registers to be modified by instructions active in a pipeline and generating a second register mask identifying registers to be modified by greater width instructions active in the pipeline, Comparing the register specifier against a second mask and comparing a register specifier against a first register mask (e.g, see figs. 13a,13b,14,25a,25b). Considering Yeager teachings of masks for determining dependency and the Prabhu teachings of dependency between single and double precision instructions one of ordinary skill would have been motivated generate register masks and to compare the double and single with register specifiers against masks (e.g., see col. 5, line 35-col. 6, line 34).

32. As to the limitations of claim 13, 14, the fetching of data in groups or blocks was well known in the art at the time of the claimed invention at least because the

instructions in the same group or block would be more likely to be to be used with a fetched instruction. Therefore it would have been obvious to one of ordinary skill that at least some instructions in the Nair and Prabhu system comprising greater and lesser width instructions that were tested as to their dependency would have been fetched in a group.

33. It would have been obvious to one of ordinary skill to combine the teachings of Prabhu and Yeager. Both references were directed toward the processing of instructions that had dependencies on other instructions. One of ordinary skill would have been motivated to incorporate the Yeager teachings of masks for comparing register modifiers at least to provide quick comparison of the register masks and providing quick determination of dependencies.

34. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Nair and Prabhu. Both references were directed to the problems of processing instructions with registers of plurality of widths (e.g., see col.3 lines 8-12 of Prabhu and col. 1, line 46-col. 2, line 18 of Nair). One of ordinary skill would have been motivated to incorporate the Nair teachings of use of register specifiers with types for indicating information such as register size in the operations at least so that the comparision of the register type would be facilitate for determining when conflicting size registers are encounters in the processing of the instruction.

Allowable Subject Matter

35. Claims 7, 32, 36 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

36. Applicant's arguments with respect to claims 1-36 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

McGrath (patent No. 7,124,286) disclosed a system establishing an operating mode in a processor (e.g., see abstract).

Rivers (patent application publication 2002/0174319) disclosed a system for reducing logic activity in a microprocessor (e.g., see abstract).

Gotou (patent No. 4,679,140) disclosed a system with control of the significant bit lengths of general purpose register (e.g., see abstract).

Guenther (patent No. 6,442,676) disclosed a processor with different width functional units ignoring extra bits of bus wider than instruction width (e.g., see abstract).

Isaman (patent No. 6,449,710) disclosed a system with stitching instructions operating on portions of a register (e.g., see abstract).

Mauhurin (patent No. 6,493,819) disclosed a system with merging narrow register for resolution of data dependencies when updating a portion of a register (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER